A GaAs MESFET 7 Gb/s DYNAMIC DECISION CIRCUIT I.C.

R. J. Bayruns, A. D. M. Chen, J. Gilbert, R. Goyal and J. Wang

ANADIGICS, INC.
35 Technology Drive
Warren, New Jersey 07060

ABSTRACT

A dynamic decision circuit uses 0.5 um gate GaAs MESFET technology and charge cancelling techniques to obtain a 7 Gb/s clocking rate. The 0.6Vp-p output data eye is symetrical and has 70 pS rise and fall times while retiming a noisy data input. The circuit operates from a single -6V supply and dissipates 0.24W of power. The chip size is 0.5 mm^2.

INTRODUCTION

High speed digital communication systems require flip-flops or decision circuits to retime data which has both amplitude and time variations. The fastest reported decision circuits to date, operate at a rate of up to 5 Gb/s.[1][2]

In this paper, we report a GaAs MESFET dynamic decision circuit which has been operated at up to 7 Gb/s. A block diagram of the flip-flop is shown in Figure 1a and a detailed schematic diagram is shown in Figure 1b. The circuit consists basically of two differential amplifiers and two sample and hold gates operating similar to a master slave D flip-flop.

Transistors M1 through M6 form the input differential amplifier of Figure 1a. Transistor M7 is the first sample and hold gate. Transistors M8 and M9 form a source follower buffer. Transistor M10 is the second sample and hold gate. The output differential amplifier is formed by transistors M11 through M16. The output impedance of M15 is about 70 ohms and is adequate to drive 0.6Vp-p across a 50 ohm load. Capacitors C1 and C3 are used to improve the bandwidth of the differential gain stages. The voltage gain of the diff amps is about 5 and the 3dB bandwidth is about 6GHz. Capacitors C2 and C4 are bypass capacitors for the DC reference voltage input.

Transistors M7 and M10 act as sampling gates and have the familiar problem of a voltage offset step when the transistor is turned off resulting in clock feedthrough at the output. For this reason, charge cancelling capacitors CC1 and CC2 are connected to the corresponding opposite phase of the clock. The value of 0.03 pf for CC1 and CC2 is about half the Cgs of M7 and M10.

CIRCUIT RESULTS

Figure 2 shows a photomicrograph of the dynamic decision circuit chip. The chip size is 700 um x 700 um.

The circuit was fabricated applying ANADIGICS' 0.5 micron gold-plated refractory-metal gate D-MESFET technology. The FETs have a pinchoff voltage of -1.4V, a transconductance of 140 mS/mm and a minimum f_t (gm/2 π Cgs) of 21 GHz. All capacitors are MIM capacitors which use Si_3N_4 as the dielectric and have a capacitance per unit area of 360 pf/mm^2. The level shifting diodes are Schottky barrier.

The circuits were packaged in a commercially available 8 lead flat pack. Since the positive supply is ground and the negative supply is connected to current source transistors, very little supply bypassing is needed.

For high frequency testing, an external 50 ohm termination resistor R_1 and 500 ohm bias resistor R_2 and R_3 are used as shown in Figure 1b. A 0.1uf capacitor is also used to enable a good 50 ohm D input match down to about 30 KHz.

The D input, reference, and clock inputs were all biased at half of VSS (-3V). The two phase clocks are generated by a 180^o 3db microwave splitter. The nominal clock amplitude needed at ϕ_1 and ϕ_2 is about 1.5Vpp. The internal 1K ohm resistor R_1 is used to feed the -3V bias to ϕ_2. The -3V bias at ϕ_1 is provided by a microwave bias tee. The nominal input data sensitivity level is about 0.3Vpp. The supply voltage on VSS is not critical because of the source coupled circuit configuration. We found the circuit operates properly from VSS = -5V to VSS = -8V. The typical offset voltage of the differential stages is 50-100mV. At -6V supply we found the common mode range to be easily $\pm$ 0.5V for D and REF inputs.

Figure 3a shows the decision circuit operation at a lower speed of 5.5 Gb/s with a clean pseudorandom NRZ input signal. The input signal was obtained by multiplexing four 1.375 pseudorandom Gb/s bit streams onto a single output. Figure 3b shows another decision circuit at 5.5 Gb/s, which does not include the charge cancelling capacitors CC1 and CC2. The output eye (top trace) is still open but has a large 5.5 GHz clock feedthrough which is not acceptable for system use.

Figure 4 shows the flip-flop retiming a noisy 7 Gb/s pseudorandom data input. The input signal (bottom trace) has an error rate of approximately 10^{-4} and the eye is barely open. The output of the decision circuit (top trace) shows a dramatic improvement in the amplitude and time jitter and has an open eye. This photo shows our decision circuit does make a decision and does not produce jitter due to metastable states.

We have additionally tested the decision circuit with a 1010... pattern at a 8 GHz clock frequency and have observed proper operation. The results we have presented here represent the highest speed reported for any decision circuit in any technology.

[1] D. Clawin, et al, "Silicon Bipolar Decision Circuit Handling Bit Rates Up To 5 Gb/s." IEEE, J. Lightwave Technology, Vol. LT, 5 March 1987.
[2] Y. Hosono, et al, "A 5 Gb/s GaAs Monolithic Master Slave D-Type Flip/Flop IC." 1987 IEEE GaAs IC Symposium, October 13, 1987, Portland, Oregon.

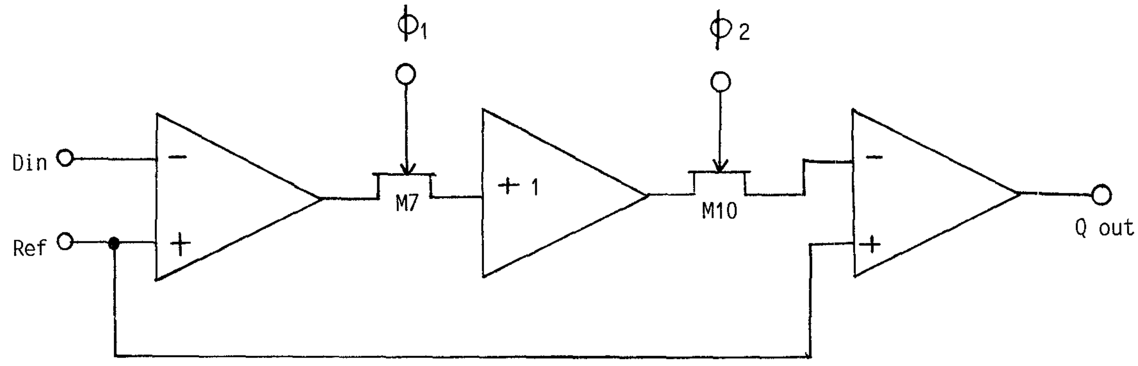

Figure 1a

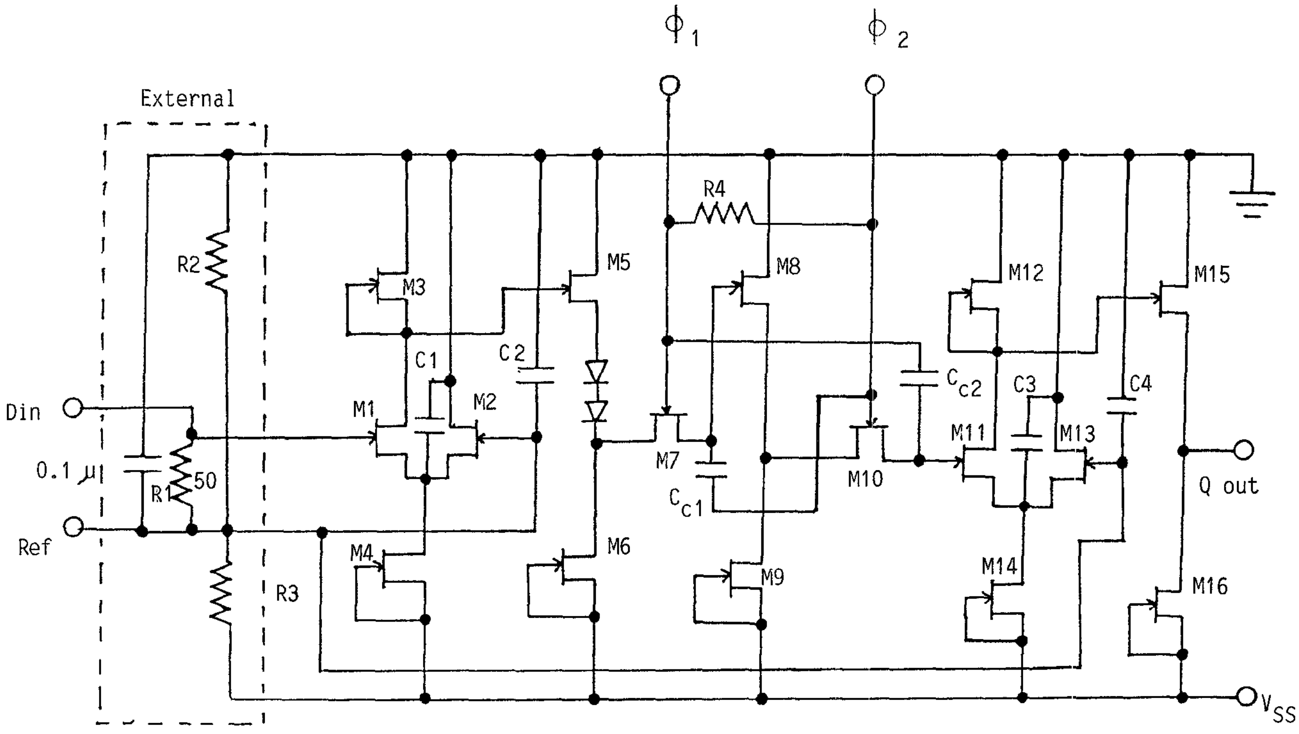

Figure 1b

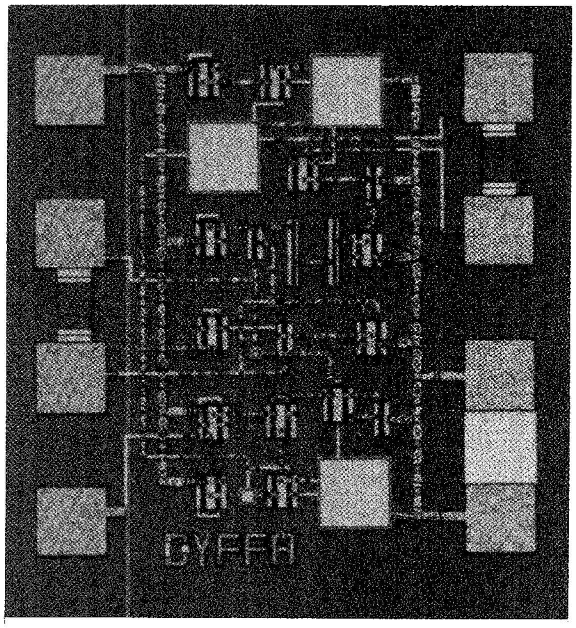

Figure 2. Dynamic Decision Circuit Chip Photo. Chip Size is 0.5 mm^2.

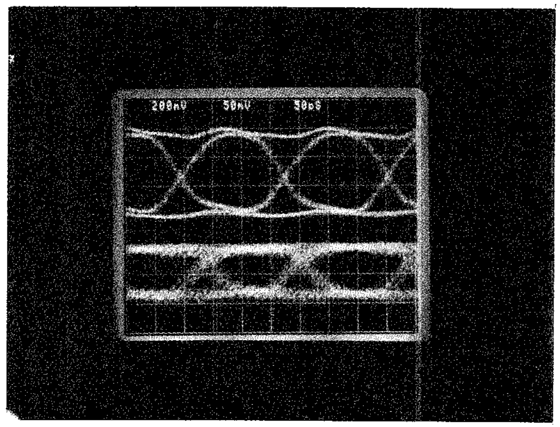

Figure 3a. Bottom Trace-Input .7v p-p 5.5 Gb/s 2E15-1 PRBS. Top Trace-Retimed Output.

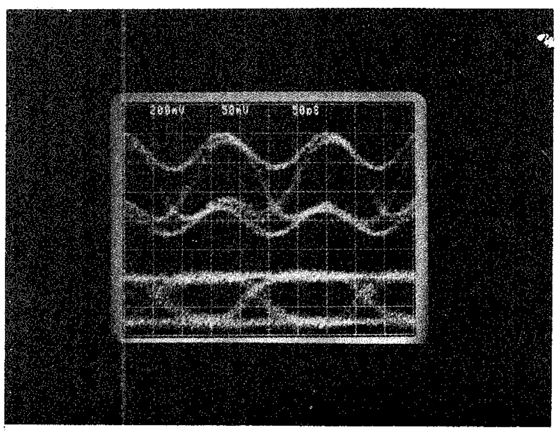

Figure 3b. Top Trace-Output of Decision Circuit with no Charge Cancelling Capacitors.

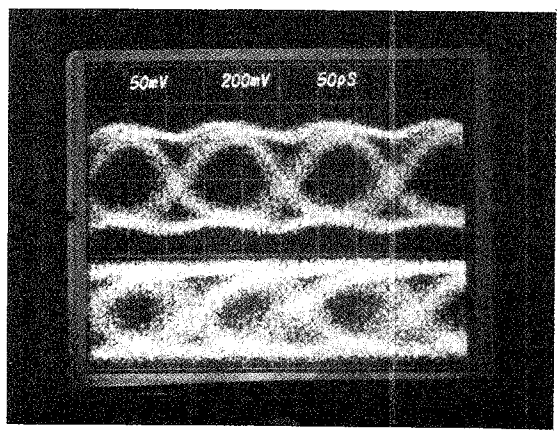

Figure 4. Bottom Trace-Input 7 Gb/s 2E15-1 PRBS, 10E-4 BER. Top Trace Retimed Output.